High Performance SOI Technology for sub-45nm gate length CMOS manufacturing

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ABSTRACT

Partially depleted (PD) SOI technologies are mature for production of high speed, low power microprocessors. The paper will high light several challenges found during the course of development of a PD 90nm SOI technology The technology features highly advanced transistors with a gate length of sub 45nm and a nine layer low k backend. The technology is currently in use to manufacture 64bit Operton™and Athlon™ microprocessors in volume.

TRANSISTORS

The CMOS transistors are formed on wafer bonded SOI material and uses several novel techniques to boost performance. The key innovations are a unique triple spacer structure, tailored junctions and stressed overlayer films [1] (Fig. 1). Individually controlled multiple offset spacers (triple spacer) in combination with tailored junctions reduce the transistor source-to-drain resistance while at the same time controlling all SOI specific body voltage effects. Stressed overlayer films are simultaneously formed on NMOS and PMOS devices (dual stressed liners) and inducing tensile strain in N-Channel and compressive strain in P-Channel, achieving higher carrier mobilities. Maximum drive currents of NIDsat=960uA/um and PIDsat=480uA/um both measured at 1V and IDoff=100nA/µm and not corrected for self-heating were realized on integrated CMOS. An impressive ring oscillator (FO=1) delay of 5.5ps was achieved.

BEOL PROCESSING

The BEOL is formed by a nine layer copper technology. The backend flow uses a CVD deposited low k dielectric to provide high interconnect density and speed. Fig 2 shows the Backend hierarchy [2].

SYSTEM PERFORMANCE

System F_{max} benefits significantly from the strained Si induced by the dual stressed liners (DSL). Fig.3 shows the F_{max} enhancement of 12% for the Athlon™ 64 over a non-stressed (neutral) liner baseline [3]

CONCLUSION

A high performance 90nm CMOS technology has been developed. The technology uses a 9 layer low k BEOL and strained Si induced by overlayer films to achieve outstanding DC and Fmax performance.

REFERENCES

[1] Horstmann et al., Proc. ICICDT p. 65

[2] Greenlaw et al., Proc. IEDM 2003 p.277

[3] H.S. Yang, Horstmann et al., Proc. IEDM 2004 (in print)

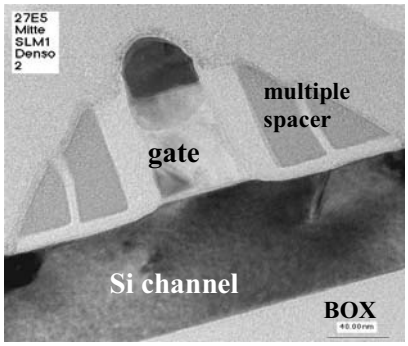

Fig. 1 X-sectional TEM of triple spacer transistor with Lg=40nm

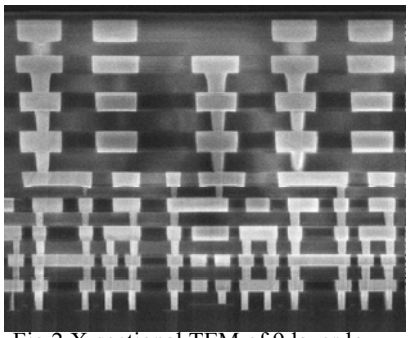

Fig.2 X-sectional TEM of 9 layer low k backend

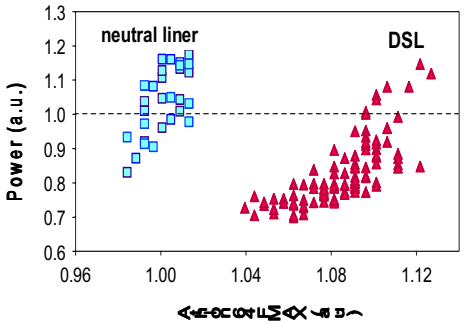

Fig.3 Athlon 64 Fmax improvement for dual stressed liner vs unstressed (neutral) liners